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Commissioner for Patents Amendment dated November 30, 2004 Response to Notice dated November 3, 2004 Page 2 of 3

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Amendments to the Specification:

Please replace the paragraph beginning at line 8, page 2, with the following:

[FIGs. 1-6] FIGs. 1-7 are cross sections of a semiconductor device according to one embodiment of the invention at selected stages in the fabrication process.

Please replace the paragraph beginning at line 28, page 6, with the following:

Shown in [FIG. 6] FIG. 7 are completed transistors 138 and 140 using gate stacks 137 and 139. Patterned photoresist portions 124 and 126 and ARC layer 122 have been removed from gate stacks 137 and 139. Transistor 138 is a P channel transistor having source/drains 142 and 144 including extension or lightly doped regions 143, a dielectric sidewall spacer and/or liner 146, and silicide regions 150, 152, and 154. Silicide regions 150 and 152 are formed over and in contact with source/drains 142 and 144, respectively. Similarly, silicide region 154 is formed over and in contact with the portion of polysilicon layer 120 that is part of the gate stack of transistor 138. Transistor 140 is an N channel transistor having source/drain regions 156 and 158 including extension or lightly doped regions 157, a dielectric sidewall spacer and/or liner 160, and silicide regions 164 and 166. Silicide regions 164 and 166 are on and in contact with source/drains 156 and 158, respectively. Also, silicide region 168 is formed over and in contact with a portion [pley] of poly layer 120 that is part of the gate stack of transistor 140 as shown in [FIG. 6] FIG. 7.